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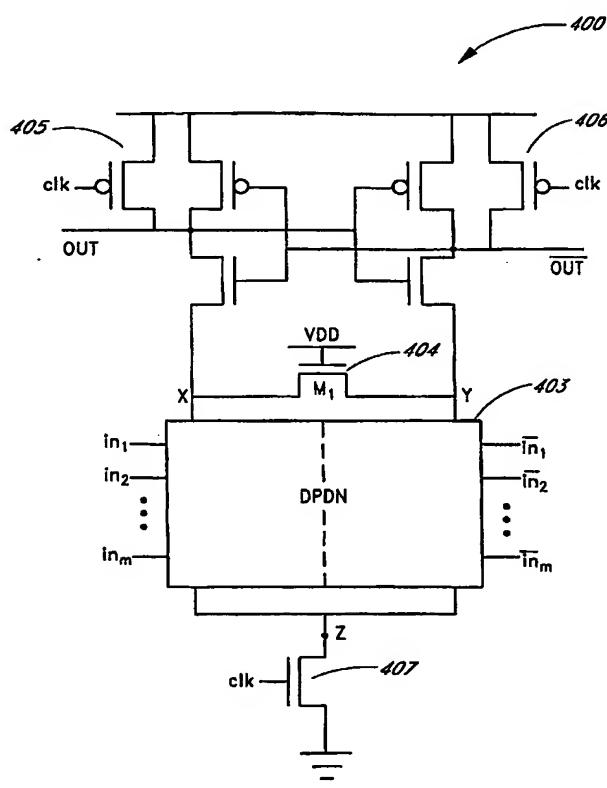
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(54) Title: A DYNAMIC AND DIFFERENTIAL CMOS LOGIC WITH SIGNAL-INDEPENDENT POWER CONSUMPTION TO WITHSTAND DIFFERENTIAL POWER ANALYSIS



(57) Abstract: A dynamic and differential CMOS logic style is disclosed in which a gate uses a fixed amount of energy per evaluation event. The gate switches its output at every event and loads a constant capacitance. The logic style is a Dynamic and Differential Logic (DDL) style. The DDL style logic typically has one charging event per clock cycle and the charging event does not depend on the input signals. The differential feature masks the input value because a precharged output node is discharged during the evaluation phase. The dynamic feature breaks the input sequence: the discharged node is charged during the subsequent precharge phase.

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